Slater & Matsil, L.L.P.
BRIDGING LAW AND TECHNOLOGY
17950 Preston Road | Suite 1000 | Dallas, TX 75252

(972) 732-1001
(972) 732-9218 FAX
www.slater-matsil.com

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TO: Examiner Fahmida Rahman
Art Unit 2116

FAX NO.: 571-273-8159

TEL NO.: 972-732-1001

FROM: Benjamin E. Nise

DATE: 10/15/2008

NO. OF PAGES: 7
(including cover page)

RE: Serial Number 10/801,130
Applicant: Eggers
Title: A Synchronizer Signal Generator Device and Process for Generating a Synchronizer Signal.

MESSAGE

Dear Examiner Rahman:

In support of our upcoming telephone interview, I have attached some material for your review including a proposed response to the Final Office Action mailed September 4, 2008. To confirm, we are scheduled for a telephone interview at 1pm EDT on October 16, 2008. Please do not hesitate to contact me if you have any questions. I can be reached at 972-732-1001 or on my cell phone at 972-898-4237.

Best Regards,

Benjamin E. Nise
Registration Number 55,500

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Eggers, *et al.*	Docket No.:	QIM 2003 P 50205 US
Serial No.:	10/801,130	Art Unit:	2116
Filed:	March 16, 2004	Examiner:	Rahman, Fahmida
For:	A Synchronizer Signal Generator Device and Process for Generating a Synchronizer Signal		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Material for Examiner Interview

Dear Examiner Rahman:

I have attached some material for your review including some proposed claim amendments in response to the Office Action mailed on September 4, 2008. More particularly, what I would like to do is make sure I have claims that make it clear that the signal generator and receiving device are both physically on opposite ends of a signal line in order to overcome Harvey. (See Office Action page 10). Any suggestion you may have regarding this would be appreciated. To confirm, we are scheduled for a telephone interview at 1pm (EDT), on Thursday, October 16, 2008.

Respectfully submitted,

10/15/2008
Date

Benjamin E. Nise
Agent for Applicant
Reg. No. 55,500

SLATER & MATSIL, L.L.P.
17950 Preston Rd., Suite 1000
Dallas, Texas 75252
Tel.: 972-732-1001
Fax: 972-732-9218

In the Claims:

1. (Currently Amended) A system, comprising:

a signal generator coupled to a signal line at a first end at a first point, the signal generator generating a signal of a particular frequency;

at least one receiving device coupled to the signal line at a second end at a second point, the second end opposite the first end, wherein the at least one receiving device comprises a clock generator, wherein the clock generator is synchronized to the signal and generates a clock signal, wherein the clock signal comprises a frequency less than a frequency of the signal of the particular frequency, and wherein the first point and the second point are physically spaced by a distance; and

an impedance element coupled to the signal line at the first end, the impedance element comprising an impedance chosen to create a resonant condition at the first end of the signal line, wherein the resonant condition comprises a resonant frequency that essentially coincides with the frequency of the signal.

2. (Previously Presented) The system according to Claim 1, wherein the signal is essentially sinusoid.

3. (Previously Presented) The system according to Claim 1, wherein the signal generator comprises a driver device.

4. (Previously Presented) The system according to Claim 1, wherein the signal generator generates an essentially rectangular signal.

5. (Previously Presented) The system according to Claim 4, wherein the essentially rectangular signal generated by the signal generator is filtered, wherein a signal present at an input node of the signal line is essentially sinusoid.

6. (Previously Presented) The system according to Claim 1, wherein the impedance element comprises an inductive component.

7. (Previously Presented) The system according to Claim 6, wherein the impedance element comprises a capacitive component.

8. (Previously Presented) The system according to Claim 7, wherein an inductance of the inductive component and/or a capacitance of the capacitive component is set during a manufacture of the system.

9. (Previously Presented) The system according to Claim 8, wherein the inductance and/or capacitance is variably adjustable after the manufacture of the system.

10. (Previously Presented) The system according to Claim 9, wherein the capacitive component comprises a capacitive diode.

11. (Previously Presented) The system according to Claim 1, wherein the at least one receiving device comprises a semi-conductor component.

12. (Previously Presented) The system according to Claim 1, wherein the at least one receiving device uses the signal for chronological co-ordination of relaying and/or processing and/or transferring of data.

13. (Previously Presented) The system according to Claim 1, wherein the at least one receiving device generates a further signal under control of the signal, wherein the further signal is used for chronological co-ordination of relaying and/or processing and/or transferring of data.

14. (Previously Presented) The system according to Claim 13, wherein the further signal comprises a lower frequency than the signal.

15. (Previously Presented) The system according to Claim 14, wherein the at least one receiving device comprises a PLL or DLL circuit, wherein the PLL or DLL circuit generates the further signal.

16. (Currently Amended) A process for generating a synchronizer, the process comprising:

transmitting a signal from a signal generator device coupled to a signal line at a first end to at least one receiving device coupled to the signal line at a second end in an electronic system, the second end opposite the first end, wherein the signal line comprises a capacitive load and the first end and second end are spaced apart by a distance;

coupling at least one additional device at an output of the signal generator, the at least one additional device comprising an impedance such that a resonant-oscillatory condition is created at the output of the signal generator device;

adjusting a center frequency of the resonant-oscillatory condition, wherein the center

frequency is modified to essentially coincide with a frequency of the signal; and

generating a clock signal synchronized to the signal, wherein a frequency of the clock signal is less than the frequency of the signal, and wherein the clock signal is generated by the at least one receiving device.

17. (Currently Amended) The process of claim 16, wherein the adjusting the center frequency comprises switching on or off at least one additional device coupled to the output of the signal generator device.

18. (Previously Presented) The process of claim 17, wherein the at least one additional device comprises a capacitive diode.

19. (Previously Presented) The process of claim 17, wherein the at least one additional device comprises at least two additional devices, the at least two additional devices being connected in parallel.

20. (Currently Amended) A system, comprising:

a first integrated circuit comprising

a signal generator coupled to an output terminal of the first integrated circuit, the signal generator generating a signal of a particular frequency, and

an impedance element coupled to the output terminal of the first integrated circuit, the impedance element comprising an impedance chosen to create a resonant condition at the output terminal, wherein the resonant condition comprises a resonant frequency that essentially coincides with a frequency of the signal of the particular frequency;

a second integrated circuit comprising a receiving device coupled to an input terminal of the second integrated circuit, wherein the receiving device comprises a clock generator, wherein the clock generator is synchronized to the signal and generates a clock signal, and wherein the clock signal comprises a frequency less than the frequency of the signal of the particular frequency; and

a signal line comprising a first end and a second end, the second end opposite the first end, wherein the first end is coupled to the output terminal of the first integrated circuit, [[and]] the second end is coupled to the input terminal of the second integrated circuit, and the first and second ends are spaced apart by a physical distance.